Low Power Mixed Signal on 16FFC

Analog Bits

ABSTRACT

Analog Bits is the leading provider of low power, mixed-signal IP with billions of IPs in production. This presentation will discuss silicon-qualified IP for TSMC's 16nm processes designed for applications such as:

• automotive

• data center

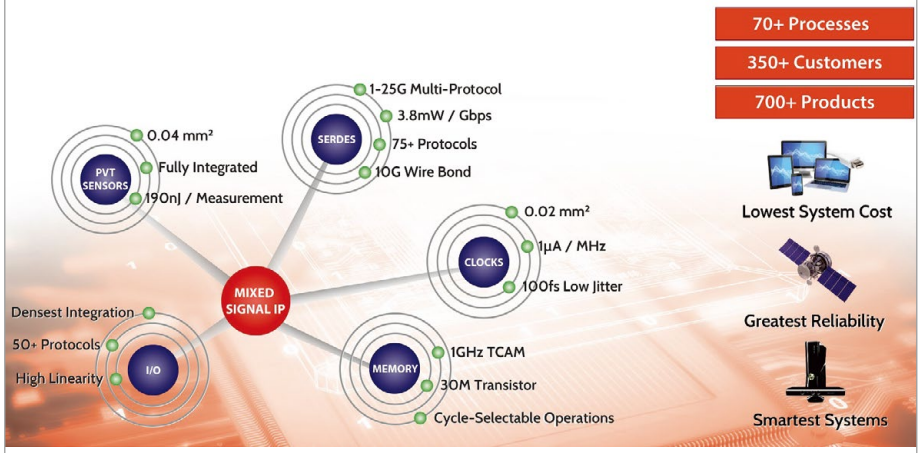
• other performance and power-sensitive developments

IP technologies discussed will include low power SERDES, PVT sensors, PLLs and other IO-related IP products. We will discuss the novel approach to keeping size small and power low and how that enables easier/faster/less risky SOC development with more flexibility on placement and lane count. All IP's discussed are silicon proven with immediate availability for high-volume deployment.

Low Power Mixed Signal on 16FFC

Silicon-proven, low power IP for TSMC 16FF+/16FFC for Automotive to Datacenter SOC's

Broadest Portfolio of Differentiated IP
Billions in Silicon



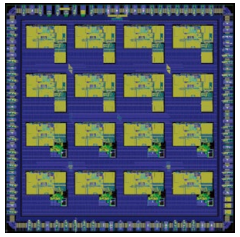
Analog Bits 16FFC IP Portfolio

- Wide Range Programmable Low Power PLL
- On-die PVT Sensor
- Power On Reset Macro for Brown Out Detection
- 1-25G Multi-rate Low Power Datacenter SERDES
- 1-10G Multi-rate Low Power Consumer/Automotive SERDES
- Clock Buffers and Programmable IO

Higher Reliability Requirements for 16FFC

- Dictated by Automotive and Datacenter
- Grade 1 Qualifications
  - High Temperature Requirements
- AEC-Q100 ESD
  - Special ESD tests needed

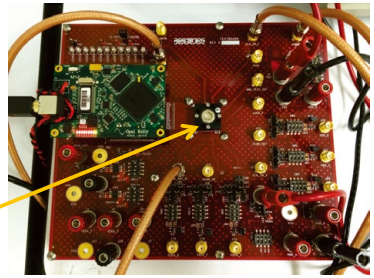
16FFC Test Chip and Device & Test Board



Test chip with 16 PLL & 16 PVT Sensor Instances

Test chip from Dec 2015 16FFC MPW Shuttle

144BGA Package



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PLL Waveform Example at Grade 2

Temperature (Tj=125C)

6.4GHz VCO with ref clock of 200/50MHz

3.2GHz VCO with ref clock of 200/50MHz

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PLL Performance Measurements at Grade 2

Conditions: VDD = 0.88V, VDDA = 1.98V, Temp (junction) = 125C

Configuration			Measured Output Results					
REF (MHz)	VCO (MHz)	Expected PLLOUT (MHz)	Frequency (MHz)	Duty Cycle (%)	Lock Time (µS)	Pk-Pk C-C Jitter (%)	Pk-Pk Period Jitter (%)	Pk-Pk TIE (%)
7	2996	23.40625	23.40625	49.9/50.0	11.17	0.30	0.23	0.19
7	5992	46.8125	46.8125	49.8/50.0	15.72	0.24	0.19	0.19
200	3200	200	200	49.1/49.8	1.78	0.64	0.42	0.60
200	6400	200	200	49.1/49.8	1.94	0.52	0.32	0.49
Spec				45/55	70	2	2	2

Conditions: VDD = 0.72V, VDDA = 1.62V, Temp (junction) = 125C

Configuration			Measured Output Results					
REF (MHz)	VCO (MHz)	Expected PLLOUT (MHz)	Frequency (MHz)	Duty Cycle (%)	Lock Time (µS)	Pk-Pk C-C Jitter (%)	Pk-Pk Period Jitter (%)	Pk-Pk TIE (%)
7	2996	23.40625	23.40625	49.8/50.0	18.61	0.28	0.21	0.24
7	5992	46.8125	46.81249	49.6/49.9	27.11	0.21	0.17	0.23
200	3200	200	200	48.3/49.4	2.17	0.72	0.47	0.77
200	6400	200	200	48.3/49.3	2.67	0.61	0.37	0.62
Spec				45/55	70	2	2	2

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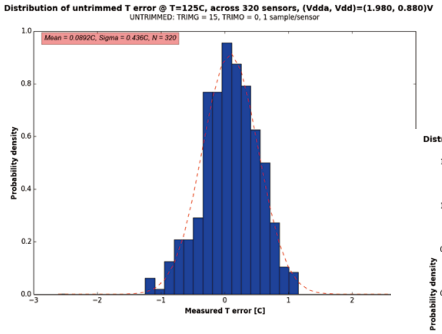
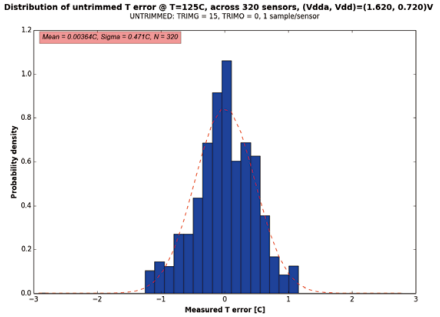
Temperature Sampling Distribution at Grade 1





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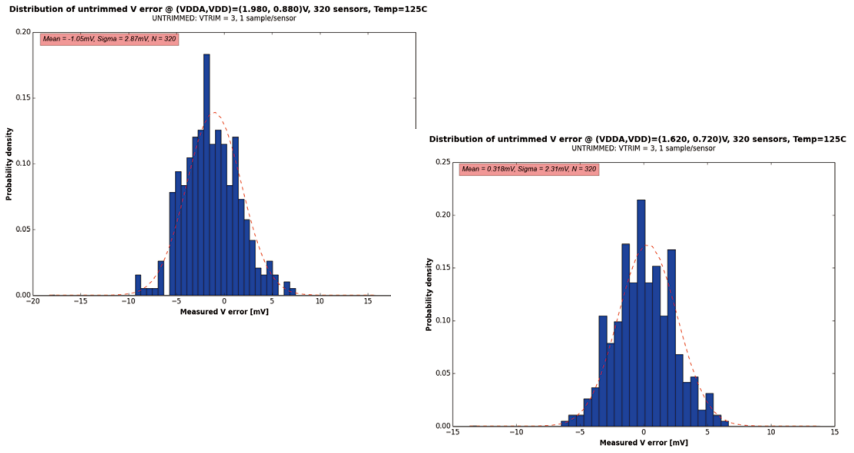
Voltage Sampling Distribution at Grade 1



Power Measurements of PLL & Sensor on 16FFC

Sensor		
	IVDDA (uA)	IVDD (uA)
Dynamic current	140	0.63
Leakage current	1.6	0.4
PLL		
	IVDDA (uA)	IVDD (uA)
Dynamic current	679	994
Leakage current	0.75	0.1

(Note: PLL operating at 6GHz VCO)

- PLL typical active power measured is 2mW (less than spec of 2.5mW max condition)
- Sensor typical active power measured is 253uW (less than spec of 320uW typical condition)

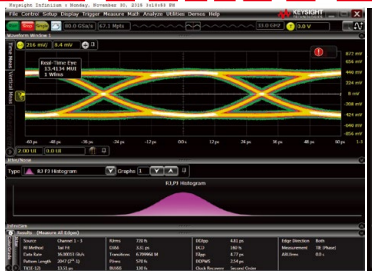
ESD Results

- HBM results pass up to +/-4KV testing
  - Passes both AEC-Q100 and JEDEC standards
- CDM results pass both AEC-Q100 and JEDEC standards
  - JEDEC testing passes up to +/-500V
  - AEC-Q100 testing passes up to +/-830V
    - Spec is +/-780V (6A)

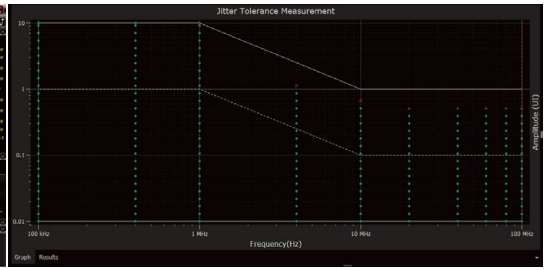
Analog Bits FinFET Development Plan

- **16FF+: 1-16G SERDES**
  - Available now (silicon proven)
  - Ready for customer tape-out
- **16FFC: 1-25G class SERDES in 16FFC**
  - Available Nov 2016
  - Test Chip Tape-out in Nov. 2016
- **16FFC: 1-10G Ultra Low Area and Low Power SERDES**
  - Available Jan 2017
  - Design Kits in Jan 2017

16FF+ SERDES Silicon Results for PCIe



16G TX Eye with Jitter Breakdown



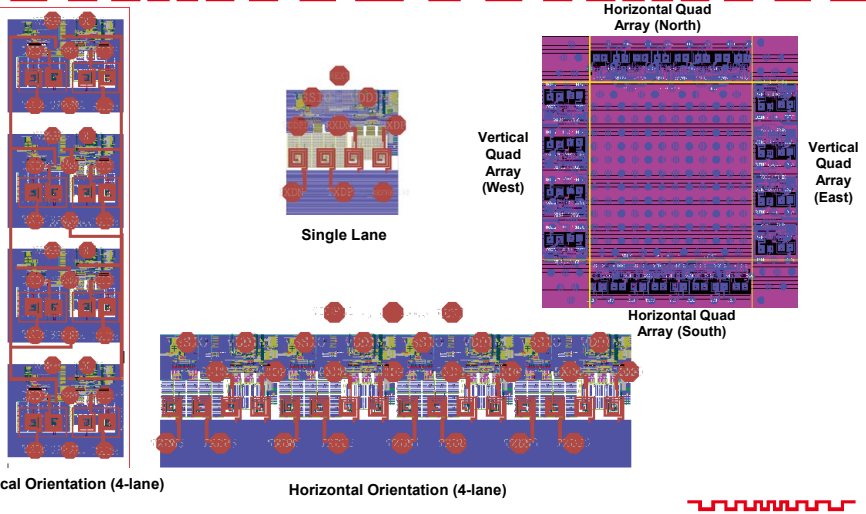
RX Jitter Tolerance @ 16G

- Flawless first silicon
- Passing PRBS in both internal and external loopback modes for 2.5G, 3G, 5G, 6G, 8G, 10G, 15G, 16G, 20G, 24G speeds

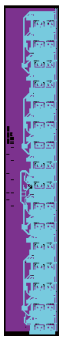
Data Rate (Gbps)	Total Power (mW/lane) (min / typ / max)	Power (mW/Gbps/lane) (min / typ / max)
5	27.05 / 34.28 / 42.54	5.41 / 6.86 / 8.51
8	39.40 / 48.58 / 61.42	4.92 / 6.20 / 7.68
16	52.17 / 68.52 / 86.56	3.26 / 4.28 / 5.41

PCI Express Power Measurements

Fully Integrated, Flexible with Multiple Orientations
allows SERDES to be placed anywhere on SOC

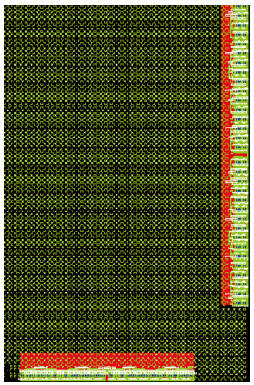


16nm SERDES integrated on DataCenter SOC
PCIe and HMC SERDES integrated on all sides of die



x16 HMC (Left Side)

x16 HMC (Left Side)



x16 HMC (Right Side)

x16 HMC (Right Side)

X16 PCIe (Bottom Side)

Case Study of 16FFC 1-10G SERDES in a Wireless VR

- SOC's are using SERDES technology to connect to Smartphones and PC's and peripherals
- Example SERDES are
  - PCIe, USB-C type
- Analog Bits 16FFC SERDES Low Power 1-10G SERDES is ideal for such applications

1-10G Multi-protocol SERDES	Power 3.8 mW/Gbps	Area: 0.12sq.mm	• Any bump pitch, 4 sides of SoC • PCIe Gen3 PCS, EPCS for SATA, USB3, etc.

Summary of 16FFC

- Analog Bits has proven silicon in 16FF+LL/16FFC
- IP's are fully functional at Grade 2 Standards
- High Performance, Low Power, SERDES for datacenters
- Low Power and Small Form Factor SERDES for automotive and consumer applications